REMARKS

This is in response to the Office Action dated July 5, 2002. Non-elected claims 13-17 have been canceled, without prejudice in view of the Restriction Requirement. New claims 18-21 have been added. Thus, claims 1-12 and 18-21 are now pending. Attached hereto is a marked-up version of the changes made to the claim(s) by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"

For purposes of example and without limitation, certain example embodiments of this invention relate to a transistor for use in a semiconductor device. A first example embodiment of the instant invention is illustrated with respect to Figures 1-4 of the application, and includes semiconductor substrate 1, first gate electrode 4 provided on the substrate with intervention of gate insulator 2, second electrode 8 provided at least partially over the first electrode 4, and a pair of spaced apart impurity regions. As shown in Figure 4, each of the impurity regions includes a low concentration impurity region 5, an intermediate concentration impurity region 9, and a high concentration impurity region 10 (source/drain). As illustrated, the low, intermediate, and high concentration impurity regions 5, 9 and 10, respectively, are sequentially arranged in this order from a region located under electrode 4 and/or 8 so that the high concentration impurity region 10 is laterally offset from and spaced apart from the low concentration impurity region 5. This arrangement of low, intermediate, and high concentration impurity regions enables the semiconductor device to have a higher breakdown voltage thereby providing for improved performance and/or reliability (e.g., page 23, lines 8-21). Moreover, the high

concentration impurity region 10 is not in contact with a portion of the substrate in which no impurity region is formed; this enables a high breakdown voltage to be achieved.

Claim 1 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Su. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes; and wherein the high concentration impurity region is laterally offset from and laterally spaced from the low concentration impurity region in said at least one impurity region." For example, see Fig. 4 of the instant application where low, intermediate and high concentration impurity regions 5, 9 and 10, respectively, are arranged in this order from a position under the gate electrode 4, and wherein the high concentration impurity region 10 is laterally offset from and laterally spaced from the low concentration impurity region 5. This is advantageous as discussed above. The cited art fails to disclose or suggest the aforesaid underlined aspect of claim 1.

Su discloses impurity regions 17, 20 and 23, and explains that impurity region 23 is highly doped, and that impurity region 17 is medium doped. The Office Action contends that region 17 is a low concentration region, while region 20 is an intermediate concentration region and region 23 is of high concentration. However, Su significantly

differs from the invention of claim 1 because in Su the high concentration impurity region 23 is not laterally offset from the alleged low concentration impurity region 17. Instead, high concentration region 23 is directly below a central portion of region 17, thereby teaching directly away from the invention of claim 1. Thus, it can be seen that Su clearly fails to disclose or suggest that "the high concentration impurity region is laterally offset from and laterally spaced from the low concentration impurity region in said at least one impurity region" as required by claim 1.

Claim 19 requires "a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes; and where a portion of the low concentration impurity region is located under at least a portion of the high concentration impurity region." For example, see Figs. 12-13 of the instant application where low concentration region 14 is located under at least a portion of high concentration region 10. The cited art fails to disclose or suggest the aforesaid underlined aspect of claim 19.

Claim 20 requires "a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes

along a horizontal direction of the semiconductor substrate." Again, Su fails to disclose or suggest this aspect of claim 20.

Claim 21 requires that "the low concentration impurity region and/or the intermediate concentration impurity region is located between (i) a portion of the substrate in which neither of the impurity regions are defined, and (ii) the high concentration impurity region, so that the high concentration impurity region is not in direct contact with the portion of the substrate in which neither of the impurity regions are defined." As explained above, this is advantageous in that a high breakdown voltage may be readily achieved.. Su fails to disclose or suggest this aspect of claim 21. Moreover, Su is undesirable in that its Su's high concentration region is located deep in the substrate and in direct contact with the portion of the substrate in which no impurity region is defined. This aspect of Su is undesirable, with respect to claim 21, in that a high breakdown voltage cannot be ensured.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claims 13-17, without prejudice in view of the Restriction Requirement.

1. (Amended) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film; [and]

a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath [the first electrode.] at least one of the first and second electrodes; and

wherein the high concentration impurity region is laterally offset from and laterally spaced from the low concentration impurity region in said at least one impurity region.

3. (Amended) A semiconductor device as set forth in claim 2, wherein the conductive layers [is] comprise silicide[films].

Please add the following new claims:

18. (New) The semiconductor device of claim 1, wherein the second electrode is a gate electrode and extends laterally beyond an edge of the first electrode.

19. (New) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film;

a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes; and

where a portion of the low concentration impurity region is located under at least a portion of the high concentration impurity region.

20. (New) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film;

a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes along a horizontal direction of the semiconductor substrate.

21. (New) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film;

a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes; and

wherein the low concentration impurity region and/or the intermediate concentration impurity region is located between (i) a portion of the substrate in which neither of the impurity regions are defined, and (ii) the high concentration impurity region, so that the high concentration impurity region is not in direct contact with the portion of the substrate in which neither of the impurity regions are defined.